

Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A circuit arrangement comprising:

a resistive-capacitive (RC) element connected between a first supply potential line and a second supply potential line, the RC element including:

a first resistor; and

a first capacitor;

a plurality of inverters connected in series and having junction points between inverters in the plurality of inverters, an input of said plurality of inverters being connected to a point between the first resistor and the first capacitor, a protection transistor having a control input, a first input, and a first output, wherein the control input is connected to the output of the plurality of inverters at a junction point, the first ~~input~~ input is connected to the first supply potential line, and the first output is connected to the second supply potential line, and a plurality of resistors, a first input of each of the resistors being connected to a different one of the junction points between the plurality of inverters and the junction point between the inverters and the protection transistor, and a second input of each of the resistors being connected to one of the first supply potential line and the second supply potential line.

2. (Previously Presented) The circuit arrangement of claim 1, wherein the resistors are alternately connected to the first supply potential line and the second supply potential line.

3. (Previously Presented) The circuit arrangement of claim 1, wherein an input of a last inverter in the plurality of inverters is connected to one of the first supply potential line and the second supply potential line by a first resistor of the plurality of resistors, and an output of the last inverter is connected to the other of the first supply potential line and the second supply potential line by a second resistor of the plurality of resistors and the output of the last inverter is connected to the control input of the protection transistor.

4. (Previously Presented) The circuit arrangement of claim 1, wherein the inverters comprise CMOS inverters.

5. (Previously Presented) The circuit arrangement of claim 1, wherein the resistors comprise diffusion resistances.

6. (Previously Presented) The circuit arrangement of claim 1, wherein the first resistor comprises a diffusion resistance.

7. (Previously Presented) The circuit arrangement of claim 1, wherein the capacitance comprises an oxide capacitance.

8. (Previously Presented) The circuit arrangement of claim 1, wherein the circuit arrangement is configured to protect integrated semiconductor circuits from electrical pulses or electrical overvoltages.

9. (Previously Presented) A circuit arrangement comprising:
a resistive-capacitive (RC) element connected between a first supply potential line and a second supply potential line, the RC element including:

a first resistor; and

a first capacitor;

a first inverter having an input and an output, wherein the input of the first inverter is connected to a first node between the first resistor and the first capacitor;

a second inverter having an input and an output, wherein the input of the second inverter is connected to the output of the first inverter at a second node;

a third inverter having an input and an output, wherein the input of the third inverter is connected to the output of the second inverter at a third node;

a protection transistor having a control input, a first input, and a first output, wherein the control input is connected to the output of the third inverter at a fourth node, wherein the first input of the protection transistor is connected to a first supply potential line, and the first output of the protection transistor is connected to a second supply potential line, and

a first resistor connected between the second node and the first supply potential line,

a second resistor connected between the third node and the second supply potential line,
and

a third resistor connected between the fourth node and the first supply potential line.

10. (Previously Presented) The circuit arrangement of claim 9, wherein the first, second, and third inverters comprise CMOS inverters.

11. (Previously Presented) The circuit arrangement of claim 9, wherein the resistors are diffusion resistances.

12. (Previously Presented) The circuit arrangement of claim 9, wherein the first resistor comprises a diffusion resistance.

13. (Previously Presented) The circuit arrangement of claim 9, wherein the capacitance comprises an oxide capacitance.